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EXAMINER	
ANGADI, MAKI A	
ART UNIT	**PAPER NUMBER**
1765	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/28/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/805,136	DAVIS ET AL.	
	Examiner	Art Unit	
	Maki A. Angadi	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *October 27th 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-21 and 36-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-21 and 36-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/20/04, 12/23/04*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 27, 2006 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35

U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

1. Claims 1-18 and 36-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fairbairn et al. (US 6,625,497) in view of Choo et al. (US 2004/0078108) and in further view of Krivokapic et al. (US 6,567,717) and Perry et al. (US 2004/0087041).

As to claims 1, 15 and 36, Fairbairn et al. discloses a semiconductor processing module with integrated feedback/feed forward metrology, wherein a method of controlling a process of fabricating integrated devices is described, the method that includes: measuring a pre-etch dimension (CD) (column 4, line 42) and a post-etch CD (column 12, line 25) of at least one structure on a substrate.

Adjusting a process recipe on an etch process (column 11, line 62) and enabling feedback to the photocell (lithography) (column 5, line 53) (column 10, line 64) or possibly photoresist trimming or shrinking (column 13, line 44) which are a capabilities for adjusting a process recipe of a pre-etch process.

Fairbairn discloses "A method and apparatus for processing a semiconductor wafer to reduce CD variation feeds back information gathered during inspection of the wafer to a previously visited processing tool and feeds forward information to adjust the next process the wafer will undergo" (abstract).

It is noted that Fairbairn is silent about the "next process" being post-etch process in particular.

The reference of Choo describes a system and methodology for monitoring and controlling a semiconductor fabrication process. Measurements are taken in accordance with scatterometry-based techniques of repeating in circuit structures that evolve on a wafer as the wafer undergoes the fabrication process. The measurements can be employed to generate feed forward and/or feedback control data that can utilized to selectively adjust one or more fabrication components and/or operating parameters associated therewith to

adapt the fabrication process (abstratct). The measurements can be utilized to generate feed forward and/or feedback control data that can utilized to selectively adjust one or more fabrication components and/or operating parameters associated therewith to achieve desired results (e.g., critical dimensions within acceptable tolerances and/or mitigation of overlay) (page 1, paragraph 0005). If not, one or more fabrication components and operating parameters associated therewith can be adapted accordingly based upon feedback/feed forward control data derived from the measurements. In one case the measurement could be performed after trench etch. For instance, the volume, degree of abrasiveness and locations of slurry selectively distributed onto the wafer and/or the degree of pressure applied between a polishing pad and the wafer during a chemical mechanical polishing (CMP) process can be adjusted to mitigate non-uniformity of the structure heights (page 5, paragraph 0042).

Choo clearly teaches measurements results (obtained after a given process step) can be used to forward-control any process step subsequent to the given step. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Fairbairn et al. to extend the feed-forward information (obtained by measuring post-etch dimensions) to adjust the next process the wafer will undergo wherein the next process includes a post-etch process because Choo teaches feed-forward control based on wafer measurements. Choo does not limit the nature of the initial process after which the measurement has been made nor does he limit

which subsequent step to control, based on those measurements, suggesting that his method can be applied to any process thereby controlling any subsequent process. One of ordinary skill in the art would have been motivated to extend the feed-forward control of Fairbairn to any post-etch process in order to correct deficiency from the lithography or the etch steps in later post-etch steps as taught by Choo. For example post-etch cleaning parameters can be adjusted if etched holes or trenches show abnormal amount of residues after the etch step.

Fairbairn et al., discloses measurement processes (col.12, lines 16-34) but is silent about a multi-pass process.

Krivokapic et al. disclose a semiconductor feed-forward control process wherein "non-conforming post-etch wafers may be returned for further etching if under-etched" (column 10, line 35), which in effect describes a multi-pass process when the under-etch is performed by design, for example when the etched layer thickness not well controlled.

The reference of Perry et al. discloses a control etch method based on an in-situ thickness measurement step.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Fairbairn et al. allowing an under-etched wafer to be re-processed or re-etched one or more than once as needed until the desired etch result is obtained which will make it a multi-pass process, the post-etched process of CD measurement will be repeated as well to

compare results with a desired CD characteristics <u>and</u> to include the thickness measurement method of Perry et al. allowing wafers which are detected to be under-etched by a post-etch measurement step to be sent back to (or remain in) the etcher for additional etching with duration determined from the differential thickness between the measured etched depth and the target etch depth, or in the method of Fairbairn et al. the CD measurement can be compared to the target waveform and if not matched, the wafer can be re-processed to match the desired profile, the process can be repeated more than once if necessary, because the methods of Krivokapic et al. and that of Perry et al. when combined with the method of Fairbairn et al. will result in further increase of yield and decrease of production cost as initially suggest by Fairbairn et al. when discussing the benefits of feedback <u>and</u> feed-forward controls (column 13, line 8). One of ordinary skill in the art would have been motivated to include a multi-pass process to the control method of Fairbairn in order to ensure process performance including the instance where some of the substrate parameters have been changed (e.g. previously deposited film quality), the controlled multi-pass method would be able to correct for such changes by automatic inspection and process adjustments.

As to claim 3, it is noted that Fairbairn is silent about detecting a failure, however, one of ordinary skill in the art would have been motivated to search and detect a failure of processing equipment, for instance, if the modified method of Fairbairn et al. yields post-etch CD measurements that are consistently out of

specification. Equipment failure detection is a routine procedure when a process fault is detected, otherwise manufacturing yield will be greatly affected.

As to claims 4, the reference of Fairbairn et al. discloses "Further exemplary embodiments of the present invention can be implemented. In these embodiments CD at the resist trim and feature etch processes (such as gate etch, shallow trench isolation (STI) trench etch, via etch, contact hole etch, metal etch, etc.) is tightly controlled using feedback and feed forward of CD measurement in real time under controlled environmental conditions" (column 13, lines 14-22). As an example a typical dual-damascene via etch is performed on a substrate including a photoresist layer, a BARC layer, a low-k dielectric, and an etch stop layer. After the BARC open step, the substrate would consist of a photoresist featured layer and a film stack (photoresist and BARC) having at least a featured layer, and a low-k blanket layer, and a film stack (low-k and etch-stop layer) having at least one blanket layer.

As to claim 5, the CD measurements suggested by Fairbairn et al., such as CD-SEM or optical inspection tool (column 4, line 58), are non-destructive measurements.

As to claim 8, Fairbairn et al. discloses a CD measurement ex-situ to the etch chamber (figure 9A-9C).

As to claims 9, 10 and 11, a CD-SEM, as described by Fairbairn, measures topographic dimensions in the same processing system including the etch chamber (figures 9A-C). It would have been obvious to one of ordinary skill

in the art at the time the invention was made to modify the method of Fairbairn, willing to transfer the wafers out of the system, to perform the CD-SEM measurement (described by Fairbairn) ex-situ in the case the CD-SEM is not integrated within the system, or move the wafers to the CD-SEM measuring station if the station is available within the system as suggested by Fairbairn, because Fairbairn teaches the benefits of the measurement (Fairbairn et al. disclose external CD measurement is conventional in the art (column 2, line 40).

As to claim 12, Fairbairn et al. describes in the "background art" section a method where the results of CD measurements are then used to adjust the etch recipe for the remaining wafers in the lot which is at least one subsequent substrate (column 3, line 6).

As to claims 53 and 13, one pre-etch process is considered to be the photo cell exposure in the method of Fairbairn et al. (column 4, line 60) performed before pre-etch dimension measurement

As to claim 14, the reference of Fairbairn et al.. describes a post etch cleaning (911) process (column 4, line 48) which could be performed after measuring the post etch measurement.

As to claim 16, the reference of Fairbairn et al. describes a a processing system including an etch chamber and a CD measurement unit (figures 9A-9C)

As to claim 17, the reference of Fairbairn et al. teaches an external CD measurement is conventional in the art (column 2, line 40).

As to claims 6, 7 and 18, Fairbairn is silent about a measuring step which is performed in-situ within the etch chamber, however, the reference teaches the benefit of performing etch and measurement within the same controlled environment thereby increasing throughput and improving yield.

The reference of Perry et al. describes an in-situ method for controlling a recess etch process wherein interferometry is used to monitor the initial thickness of a top layer or the actual etching of the recess in real time in an etch chamber (pages 3 and 4, paragraphs 0039 and 0055), the measurement system comprises a process module, data collection and a computer (figure 4A). The interferometry measurement is also conventionally used as end-point detection.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the method of Fairbairn et al. by including the etch chamber in-situ measurement system of Perry et al. because etch recess measurement is as important as CD measurement particularly when it is performed within the etch chamber for manufacturing process control and reliability of the final product. One of ordinary skill in the art would have been motivated to use an etch recess measurement for process controllability in order to detect under-etching or over-etching before the wafer leaves the etched chamber.

As to claim 37, it would be obvious to one of ordinary skill in the art to expect some kind of a failure if the target CD waveform or depth is not achieved

after the final inspection step . Detecting equipment failure would be the first obvious trouble-shooting step.

As to claim 38, Fairbairn discloses "Further exemplary embodiments of the present invention can be implemented". In these embodiments CD at the resist trim and feature etch processes (such as gate etch, shallow trench isolation (STI) trench etch, via etch, contact hole etch, metal etch, etc.) is tightly controlled using feedback and feed forward of CD measurement in real time under controlled environmental conditions" (column 13, lines 14-22). As an example a typical dual-damascene via etch is performed on a substrate including a photoresist layer, a BARC layer, a low-k dielectric, and an etch stop layer. After the BARC open step, the substrate would consist of a photoresist featured layer and a film stack (photoresist and BARC) having at least a featured layer, and a low-k blanket layer, and a film stack (low-k and etch-stop layer) having at least one blanket layer.

As to claim 39, none of the measurements cited in the references above are destructive.

As to claim 40, 41, Fairbairn et al. is silent about a measuring step which is performed in-situ within the etch chamber, however, the reference teaches the benefit of performing the etch and measurement within the same controlled environment thereby increasing throughput and improving yield.

Perry et al. describes an in-situ method for controlling a recess etch process wherein interferometry is used to monitor the initial thickness of a top

layer or the actual etching of the recess in real time in an etch chamber (pages 3 and 4, paragraphs 0039 and 0055), the measurement system comprises a process module, data collection and a computer (figure 4A). The interferometry measurement is also conventionally used as end-point detection.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the method of Fairbairn et al. by including the etch chamber in-situ measurement system of Perry et al. because etch recess measurement is as important as CD measurement particularly when it is performed within the etch chamber for manufacturing process control and reliability of the final product. One of ordinary skill in the art would have been motivated to use an etch recess measurement for process controllability in order to detect under-etching or over-etching before the wafer leaves the etched chamber.

As to claim 42, Fairbairn et al. discloses a CD measurement ex-situ to the etch chamber (figure 9A-9C).

As to claims 43-45, a CD-SEM, as described by Fairbairn, measures topographic dimensions in the same processing system including the etch chamber (figures 9A-C). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Fairbairn, willing to transfer the wafers out of the system, to perform the CD-SEM measurement (described by Fairbairn) ex-situ in the case the CD-SEM is not integrated within the system, or move the wafers to the CD-SEM measuring station if the station is

available within the system as suggested by Fairbairn, because Fairbairn teaches the benefits of the measurement (Fairbairn et al. disclose external CD measurement is conventional in the art (column 2, line 40).

As to claim 46, Fairbairn describes in the "background art" section a method where the results of CD measurements are then used to adjust the etch recipe for the remaining wafers in the lot which is at least one subsequent substrate (column 3, line 6).

As to claim 47, one pre-etch process is considered to be the photo cell exposure in the method of Fairbairn et al. (column 4, line 60) performed before pre-etch dimension measurement

As to claim 48, Fairbairn et al. describes a post etch cleaning (911) process (column 4, line 48) which could be performed after measuring the post etch measurement.

As to claim 49, Fairbairn et al. discloses a semiconductor processing module with integrated feedback/feed forward metrology wherein a method of controlling a process of fabricating integrated devices is described, the method comprises: measuring a pre-etch dimension (CD) (column 4, line 42) and a post-etch CD (column 12, line 25) of at least one structure on a substrate and adjusting a process recipe on an etch process (column 11, line 62) and enabling feedback to the photocell (lithography) (column 5, line 53) (column 10, line 64) or possibly photoresist trimming or shrinking (column 13, line 44) which are a capabilities for adjusting a process recipe of a pre-etch process.

Fairbairn discloses "A method and apparatus for processing a semiconductor wafer to reduce CD variation feeds back information gathered during inspection of the wafer to a previously visited processing tool and feeds forward information to adjust the next process the wafer will undergo" (abstract). It is noted that Fairbairn is silent about the "next process" being a post-etch process in particular.

The reference of Choo describes a system and methodology for monitoring and controlling a semiconductor fabrication process. Measurements are taken in accordance with scatterometry-based techniques of repeating in circuit structures that evolve on a wafer as the wafer undergoes the fabrication process. The measurements can be employed to generate feed forward and/or feedback control data that can utilized to selectively adjust one or more fabrication components and/or operating parameters associated therewith to adapt the fabrication process (abstratct). The measurements can be utilized to generate feed forward and/or feedback control data that can utilized to selectively adjust one or more fabrication components and/or operating parameters associated therewith to achieve desired results (e.g., critical dimensions within acceptable tolerances and/or mitigation of overlay) (page 1, paragraph 0005). If not, one or more fabrication components and operating parameters associated therewith can be adapted accordingly based upon feedback/feed forward control data derived from the measurements. In one case the measurement could be performed after trench etch. For instance, the volume, degree of abrasiveness

and locations of slurry selectively distributed onto the wafer and/or the degree of pressure applied between a polishing pad and the wafer during a chemical mechanical polishing (CMP) process can be adjusted to mitigate non-uniformity of the structure heights (page 5, paragraph 0042).

Choo clearly teaches measurements results (obtained after a given process step) can be used to forward-control any process step subsequent to the given step. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Fairbairn et al. to extend the feed-forward information (obtained by measuring post-etch dimensions) to adjust the next process the wafer will undergo wherein the next process includes a post-etch process because Choo teaches feed-forward control based on wafer measurements. Choo does not limit the nature of the initial process after which the measurement has been made nor does he limit which subsequent step to control, based on those measurements, suggesting that his method can be applied to any process thereby controlling any subsequent process. One of ordinary skill in the art would have been motivated to extend the feed-forward control of Fairbairn to any post-etch process in order to correct deficiency from the lithography or the etch steps in later post-etch steps as taught by Choo. For example post-etch cleaning parameters can be adjusted if etched holes or trenches show abnormal amount of residues after the etch step. As to claim 50, see discussion for claim 16 above.

As to claim 51, Fairbairn et al. teaches an external CD measurement is conventional in the art (column 2, line 40).

As to claim 52, Fairbairn et al. is silent about a measuring step which is performed in-situ within the etch chamber, however, the reference teaches the benefit of performing etch and measurement within the same controlled environment thereby increasing throughput and improving yield.

Perry et al. describes an in-situ method for controlling a recess etch process wherein interferometry is used to monitor the initial thickness of a top layer or the actual etching of the recess in real time in an etch chamber (pages 3 and 4, paragraphs 0039 and 0055), the measurement system comprises a process module, data collection and a computer (figure 4A). The interferometry measurement is also conventionally used as end-point detection.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the method of Fairbairn et al. by including the etch chamber in-situ measurement system of Perry et al. because etch recess measurement is as important as CD measurement particularly when it is performed within the etch chamber for manufacturing process control and reliability of the final product. One of ordinary skill in the art would have been motivated to use an etch recess measurement for process controllability in order to detect under-etching or over-etching before the wafer leaves the etched chamber.

Claim Rejections - 35 USC § 103

2. Claims 19-21 are rejected under 35 U.S.C. 103(a) as being obvious over Fairbairn et al. (US 6,625,497) in view of Choo et al. (US 2004/0078108), Krivokapic et al. (US 6,567,717) and Perry et al. (US 2004/0087041) as applied to claim 1 above, and in further view of Morgenstern (US 2003/0022510)

Fairbairn discloses a trench etch (column 13, lines 14-22), but fails to specifically disclose a trench capacitor.

The reference of Morgenstern (US 2003/0022510) teaches a formation of a capacitive trench structure with a polysilicon electrode layer wherein the etch process is performed with an HBr and Cl2 chemistry (page 2, paragraphs 0033-0035). The flow rate of $HBr:Cl_2$ is 45:135 or 1:3 (page 3, paragraph 0044).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the method of Fairbairn et al. by including a capacitive trench structure with a polysilicon electrode layer wherein the etch process is performed with an HBr and Cl_2 chemistry because the reference of Fairbairn et al. teaches the disclosed control method is applicable to any structure. One of ordinary skill in the art would be motivated to apply the method of Fairbairn et al. to a capacitive structure in order to control the capacitance characteristics and values with a high precision from wafer-to-wafer in a manufacturing environment.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Maki A. Angadi whose telephone number is 571-272-8213. The examiner can normally be reached on 8 AM to 4.30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Dr. Maki Angadi
Examiner
Art Unit 1765

SHAMIM AHMED
PRIMARY EXAMINER